REMARKS

Initially, Applicant would like to thank the Examiner for acknowledging consideration of each of the documents cited in the Information Disclosure Statements filed on February 19, 2002 and November 21, 2005. Applicant would also like to thank Supervisory Patent Examiner Fan for his courtesy in discussing the prosecution history of the present application with Applicant's representative, Joshua M. Povsner, on August 29, 2006 via teleconference. In this regard, Applicant's representative noted that claims of the present application have now been twice indicated as allowable and later rejected. Applicant's representative expressed particular concern that rejected claims were cancelled in order to obtain early allowance of claims indicated as allowable, only to have the claims indicated as allowable later subject to new rejections. The Supervisory Patent Examiner agreed to discuss the prosecution history of the present application with the Examiner when the Examiner returns from vacation.

In the outstanding Official Action, claim 15 was rejected over SATO (U.S. Patent No. 5,956,328) in view of the Admitted Prior Art and OMORI (U.S. Patent No. 6,239,666). Applicant traverses the outstanding rejection of claim 15. In this regard, claim 15 recites:

A signal point mapping circuit for mapping a QPSK modulation signal in a phase space, comprising:

a sign inversion circuit that performs a sign inversion of the QPSK modulation signal to a phase offset of a multiple of 90°;

an amplitude adjustment circuit that adjusts the amplitude of the signal output

from the sign inversion circuit and outputs a phase offset signal; and

a phase offset circuit that performs a phase offset calculation smaller than 90° with the phase offset signal output from the amplitude adjustment circuit, said phase offset circuit comprising a fixed phase offset circuit that provides a predetermined amount of a fixed phase offset,

wherein said phase offset circuit decides whether to provide the phase offset to an input signal with the fixed phase offset circuit, and

wherein said phase offset circuit controls a total phase offset amount with the phase offset implemented by the sign inversion circuit to become a desired offset amount.

The combination recited in claim 15 is not disclosed, suggested or rendered obvious by any proper combination of SATO, the Admitted Prior Art and/or OMORI. Rather, at cols. 4-5, SATO discloses a pi/4 shift QPSK spreading circuit 102. As shown in FIG. 1, pi/4 shift QPSK spreading circuit 102 includes phase shifter 201 and phase shifter 202. Phase shifter 201 "is a QPSK spreading circuit which selects a phase shift amount" from 0, +pi/2, -pi/2 and pi depending on a two-bit spreading code (see col. 4, lines 59-62). Phase shifter 202 "selects a phase shift amount" from 0 and pi/4 according to an even-odd discrimination clock signal. Phase shifter 202 shifts a phase of data output from phase shifter 201 (see col. 5, lines 1-5). Although not entirely clear, it appears that the rejection of claim 15 is based on the assertion that phase shifter 201 in SATO discloses the "sign inversion circuit" recited in claim 15, and that phase shifter 202 in SATO discloses the "phase offset circuit" recited in claim 15.

Even if the above-noted interpretation of SATO were taken as true, SATO fails to disclose the "amplitude adjustment circuit" recited in claim 15. SATO further fails to disclose that phase shifter 202 "performs a phase offset calculation... with the phase offset signal output from the amplitude adjustment circuit" as recited in claim 15. SATO moreover fails to disclose that phase shifter 202 "controls a total phase offset amount with the phase offset implemented by the sign inversion circuit to become a desired offset amount" as recited in claim 15.

Accordingly, it would be necessary to provide SATO with extensive modifications to remedy the above-noted shortcomings in order to obtain the combination recited in claim 15. However, there is no proper explanation in the Official Action as to how or why such extensive modifications would be made to SATO. In this regard, there is no proper motivation to modify SATO in the extensive manner necessary to obtain the combination recited in claim 15. Rather, the only motivation to modify SATO in the extensive manner necessary to obtain the combination recited in claim 15 is the improper motivation to obtain Applicant's claims in hindsight.

The Official Action acknowledges that SATO fails to disclose the "amplitude adjustment circuit" recited in claim 15, and it would follow that SATO also fails to disclose that phase shifter 202 "performs a phase offset calculation... with the phase offset signal output from the amplitude adjustment circuit" as recited in claim 15. The Official Action asserts that the Admitted Prior Art discloses "an amplitude adjustment circuit that adjusts the amplitude of the phase offset signal before the phase-offset calculator (Fig. 4B, means 406 and 407)", and that it would be obvious to modify SATO to include such an amplitude adjustment circuit. However, FIG. 4B of the Admitted Prior Art does not show that an

amplitude adjustment circuit "adjusts the amplitude of the signal output from the sign inversion circuit and outputs a phase offset signal" (emphasis added) as recited in claim 15.

Further, there is no proper motivation to place such an amplitude adjustment circuit between phase shifter 201 and phase shifter 202 in SATO insofar as the Admitted Prior Art shown in FIG. 4B explicitly discloses that amplitude adjustment occurs before phase offset. Accordingly, even the modification of SATO with the Admitted Prior Art shown in FIG. 4B would result in the amplitude adjustment circuit being placed before phase shifter 201 and phase shifter 202 in SATO.

Therefore, even modification of the teachings of SATO would not result in "an amplitude adjustment circuit that adjusts the amplitude of the signal output from the sign inversion circuit" or that phase shifter 202 would perform "a phase offset calculation... with the phase offset signal output from the amplitude adjustment circuit" as recited in claim 15.

SATO moreover fails to disclose that phase shifter 202 "controls a total phase offset amount with the phase offset implemented by the sign inversion circuit to become a desired offset amount" as recited in claim 15. In this regard, the Official Action asserts that SATO discloses these features at col. 5, lines 37-60, Table II and phase shifter 202. However, at col. 5, lines 37-60, SATO discloses that the phase shifting operation is performed "according to the even-odd discrimination clock signal CLK 3 as shown in the following table II". Accordingly, in those portions of SATO cited in the Official Action, SATO is not controlling a total phase offset amount "to become a desired offset amount" as recited in claim 15. Further, these features are also not disclosed or suggested by the Admitted Prior Art or any other reference of record, nor does the Official Action assert that

these features are disclosed or suggested by the Admitted Prior Art or any other reference of record.

Finally, the Official Action asserts that it would be obvious to modify SATO with teachings of OMORI purportedly directed to a "modulator that uses a sign inversion circuit to invert the signal of the input signed binary data and adjusts the amplitude of the phase offset signal after the sign inversion". It is not clear why the Examiner believes one of ordinary skill in the art would use such teachings in OMORI to further modify SATO. In this regard, it appears that the rejection of claim 15 is based on an interpretation that the phase shifter 201 of SATO already discloses the "sign inversion circuit" recited in claim 15.

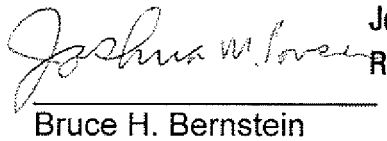
Accordingly, at least for each and all of the numerous reasons set forth above, claim 15 is not disclosed, suggested or rendered obvious by the Admitted Prior Art and the documents applied in the outstanding Official Action. Therefore, Applicant respectfully requests reconsideration and withdrawal of the rejection of claim 15, as well as an indication of the allowability of claim 15.

SUMMARY AND CONCLUSION

The present application is believed to be in condition for allowance. Applicant has explained how the combination of features recited in the pending claim are not disclosed, suggested or rendered obvious by the documents applied in the Official Action. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the outstanding rejection, and an indication of the allowability of the claim now pending.

Should the Examiner have any questions, please contact the undersigned at the telephone number provided below.

Respectfully submitted,
Kazayuki OHHASHI



Joshua M. Povsner
Reg. #42,086

Bruce H. Bernstein
Reg. No. 29,027

September 1, 2006
GREENBLUM & BERNSTEIN, P.L.C.
1950 Roland Clarke Place
Reston, VA 20191
(703) 716-1191